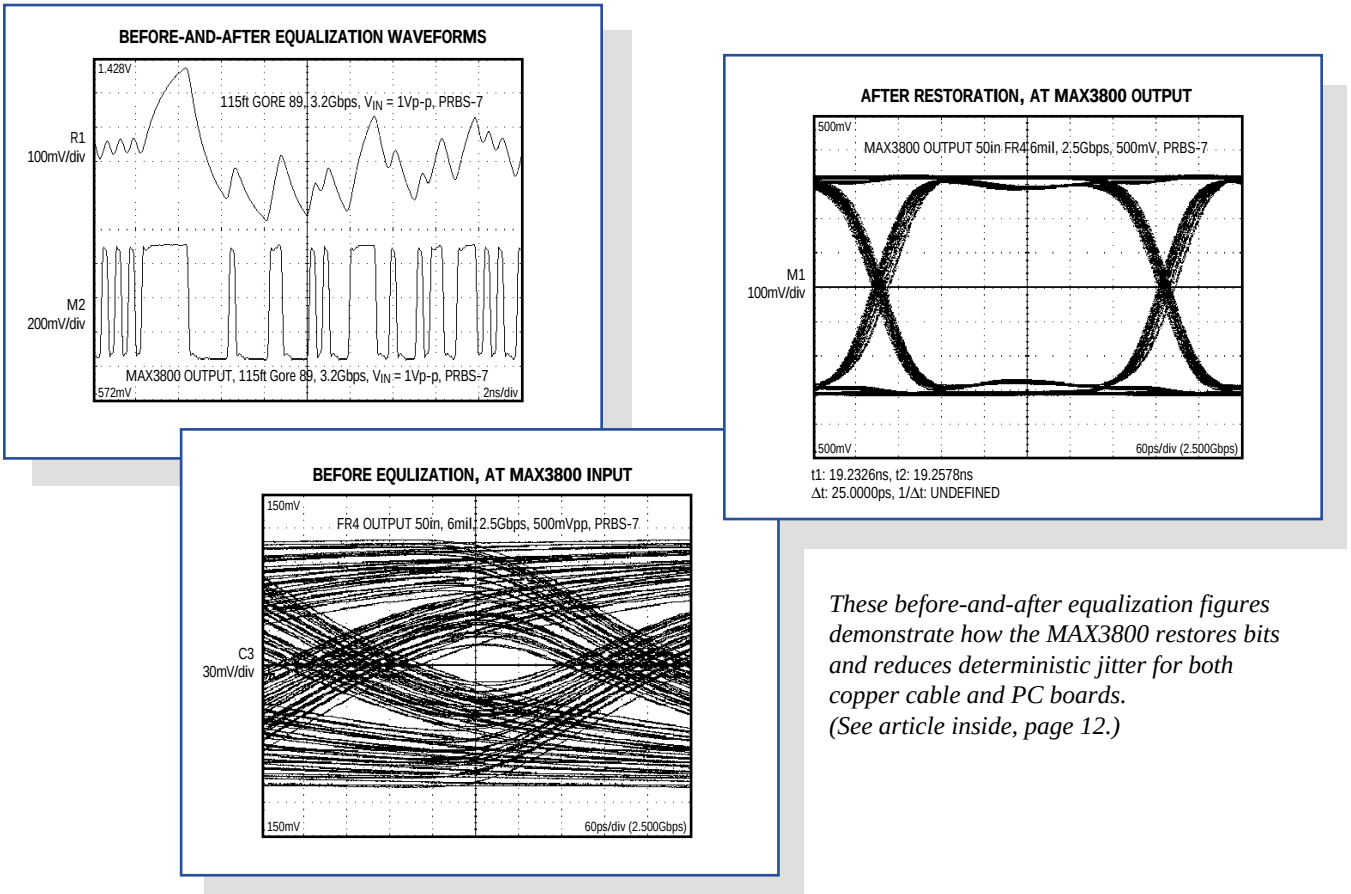
MAXIM Engineering Journal

Volume Forty-Two



These before-and-after equalization figures demonstrate how the MAX3800 restores bits and reduces deterministic jitter for both copper cable and PC boards.
(See article inside, page 12.)

News Briefs

MAXIM REPORTS RECORD REVENUES AND EARNINGS FOR THE SECOND QUARTER OF FISCAL 2001

Maxim Integrated Products, Inc., (Nasdaq: MXIM) reported record net revenues of $305.1 million for its fiscal second quarter ending December 30, 2000, a 51.2% increase over the $201.7 million reported for the same quarter a year ago. Net income increased to a record $99.1 million in the second quarter, compared to $64.6 million last year, a 53.3% increase. Diluted earnings per share were $0.31 for the second quarter, a 55.0% increase over the $0.20 reported for the same period a year ago.

During the quarter, cash and short-term investments increased by $44.6 million after paying $103.1 million for 1.7 million shares of the Company's common stock and $60.2 million for property and equipment. Accounts receivable decreased by $17.1 million to $127.4 million. Although revenues increased significantly, inventories decreased to $63.5 million during the quarter. Gross margin for the second quarter was 70.6%, compared to 70.5% in the first quarter of fiscal 2001. Research and development expense was $51.3 million or 16.8% of net revenues in the second quarter, compared to $46.7 million or 16.4% of net revenues in the first quarter. During the quarter, the Company increased inventory reserves by $14.3 million and recorded a writedown of property and equipment of $11.6 million to cost of goods sold and $3.6 million to research and development expense. Additionally, the Company recorded a $4.0 million charge to selling, general and administrative expense primarily related to technology licensing matters.

End market bookings in the second quarter of fiscal 2001 were $332 million, down slightly (5%) from first quarter end market bookings of $348 million. U.S. distributor bookings on Maxim were 28% below bookings received from their customers. This was in part due to our encouraging them to manage inventory of our product at their locations. As a result, second quarter bookings on Maxim were $308 million, compared to $339 million for the first quarter of the fiscal year. We believe that end market consumption remains in line with our projection for the fiscal year.

Turns orders received in the quarter were $58 million, compared to $98 million received in the prior quarter (turns orders are customer orders that are for delivery within the same quarter and may result in revenue within the same quarter if the Company has available inventory that matches those orders). End market bookings decreased in the U.S. and Pacific Rim, but increased in both Europe and Japan. Bookings were lower in the notebook and cell phone end markets, where there appears to be an inventory correction underway.

Second quarter ending backlog shippable within the next 12 months was approximately $431 million, including approximately $330 million requested for shipment in the third quarter of fiscal 2001. The Company's first quarter ending backlog shippable within the next 12 months was approximately $443 million, including approximately $353 million that was requested for shipment in the second quarter. All of these backlog numbers have been adjusted to be net of cancellations and estimated future U.S. distribution ship and debit pricing adjustments.

Jack Gifford, Chairman, President, and Chief Executive Officer, commented on the results: "We had excellent results during the second quarter, with continued record revenues and earnings. Quarterly bookings continue to moderate as customers and distributors, primarily in the U.S. and Pacific Rim, adjust their ordering patterns. While this trend may continue through the third quarter, we believe that the end market consumption for our products continues to support our revenue and earnings outlook for the fiscal year. We are comfortable with our backlog level, particularly since approximately 90% of our backlog is composed of proprietary products."

Mr. Gifford concluded: "We are making good progress toward meeting our goal of introducing over 450 products this year. We are now halfway through our product announcement year and have introduced 246 products. We remain focused on releasing excellent new products to the marketplace that will enable us to meet our 5-year plans. The recently announced acquisition plan for Dallas Semiconductor will certainly add to our new product efforts during this period."

Isolated power supply for telecom/datacom applications

One challenge facing modern electronic circuits is the power-supply requirement. With ever-increasing functionality and density, the challenge remains concerning how to power these high-performance boards in the most cost-effective and efficient way. But these two basic requirements are contradictory in many systems. A third requirement that adds to the complexity is the overall size of the power supply. Power supplies are often an afterthought, and their requirements are not set forth in great detail at the start of a project. This results in last-minute compromises that lead either to higher costs or larger systems.

Existing solutions

One solution that system integrators have devised is to use power-supply "bricks" from various established power-supply manufacturers that offer a "canned solution" to the problem. These power bricks come in off-the-shelf standard configurations, pretested, ready to use, and treated like any other component in the system (notwithstanding their size). Traditionally, these are completely potted devices; only their connection leads are exposed for soldering, and in many cases they require bulky heatsinks to cool them down effectively. Most of the time it is up to the system integrator to provide adequate cooling in the form of airflow. The drawbacks of the power bricks include long leadtimes, inflexible output voltages, and most importantly, cost.

In-house-designed power supplies

As an alternative to off-the-shelf power bricks, it is sometimes advantageous to have the power supplies designed in-house. This offers several advantages such as optimized footprint shapes for the end application, custom output voltages, and lower overall costs. However, this activity may require a dedicated group of power-supply design engineers. Design and verification times for these power supplies may not be possible given time-to-market pressures.

The in-house designing activity can be made simpler, to some extent, by the support provided by semiconductor companies that build the control IC for such power supplies. The term "off-the-shelf designs" can appropriately be used to describe these power supplies. A few semiconductor companies have opted to provide reference designs. These reference designs can greatly reduce power-supply design activity. In this example, the system integrator adopts and uses the optimized reference designs furnished by semiconductor companies like Maxim. This results in cost reductions as well as more control on the layout and placement of the power-supply components.

Telecom/datacom/server power supplies

One type of power supply currently in great demand is for telecom/datacom. These power supplies are used in central offices, PBXs, servers, and generally wherever the input voltage is 36V to 72V. An important requirement for these power supplies is galvanic isolation between primary and secondary, high-efficiency over a wide input voltage range, and general ruggedness.

The design of these power supplies is relatively complex due to the requirements of isolation. Typical output power levels range from about 10W to 100W or even higher. Most brick-type power supplies serve these requirements.

A 50W isolated power supply

A 50W off-the-shelf-designed power supply is shown in **Figure 1**. This is an isolated power supply with a 5V regulated output. **Table 1** summarizes some of the target specifications.

Table 1. 50W isolated power-supply specifications

Parameter	Specification
P_{OUT}	50W
V_{IN}	+36V to +72V OR -36V to -72V
V_{OUT}	+5V
I_{OUT}	10A
Initial output voltage setpoint accuracy	±3%
Output voltage regulation	<1%, over line and load
Switching frequency	250kHz ±25%
Input output isolation	1500V for 1s

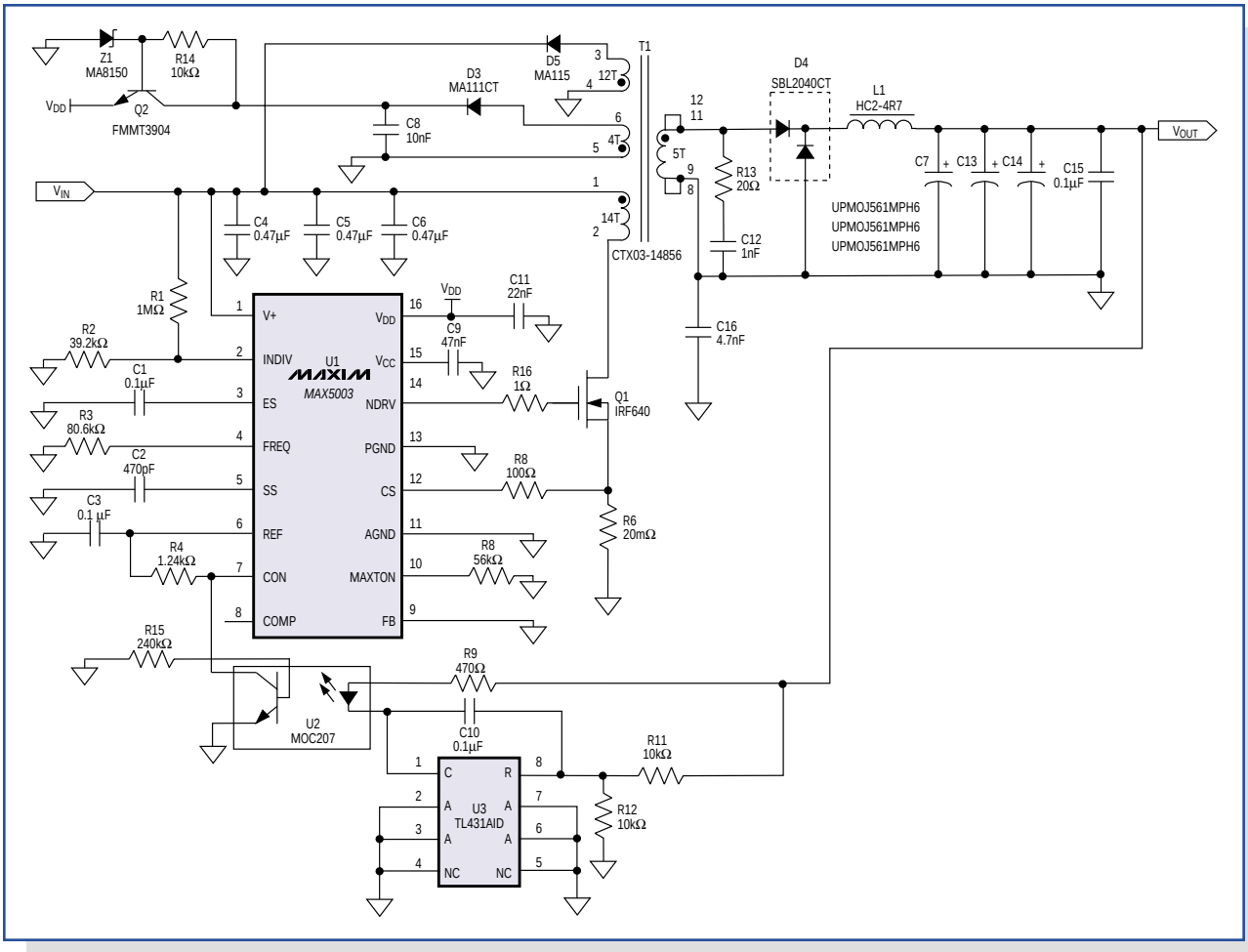


Figure 1. Schematic diagram of ±48V in and 5V out at 10A isolated power supply

Power-circuit topology

Among several power topologies available, the single-transistor forward topology offers the simplest solution and lowest cost, while at the same time providing very good efficiencies throughout the operating power range **(Figure 2a)**. This topology, however, requires a transformer reset winding connected to pins T1-3 and T1-4. The forward converter was chosen because it offers higher power density and higher efficiency than a flyback converter at these power levels. Although first-order flyback topology schematics tend to look simpler, these converters are more difficult to deal with (see sidebar for a brief comparison) **(Figure 2b)**. Transformer T1 provides the necessary isolation between primary and secondary, in this case 1500V. Efficiency is improved by powering the control circuit in the primary (T1-5, T1-6 leads) after initial startup. A 250kHz switching frequency was selected to allow for minimizing the size of energy storage components such as transformers.

The control circuit

The primary-side control circuit of Figure 1 is based on a MAX5003. **Figure 3** shows a simplified block diagram of this IC. The MAX5003 represents the next generation of power-supply controllers that integrate many functions necessary for the design of telecom power supplies. The device contains a high-voltage startup circuit that speeds the initial power-up process. It also has other facilities that ease the design of isolated, regulated telecom power supplies, such as voltage feedforward compensation. Voltage feedforward is an important element of the design because it helps to provide constant power-stage gain that results in more stable voltage control loops. Voltage feedforward also significantly helps with input supply rejection by

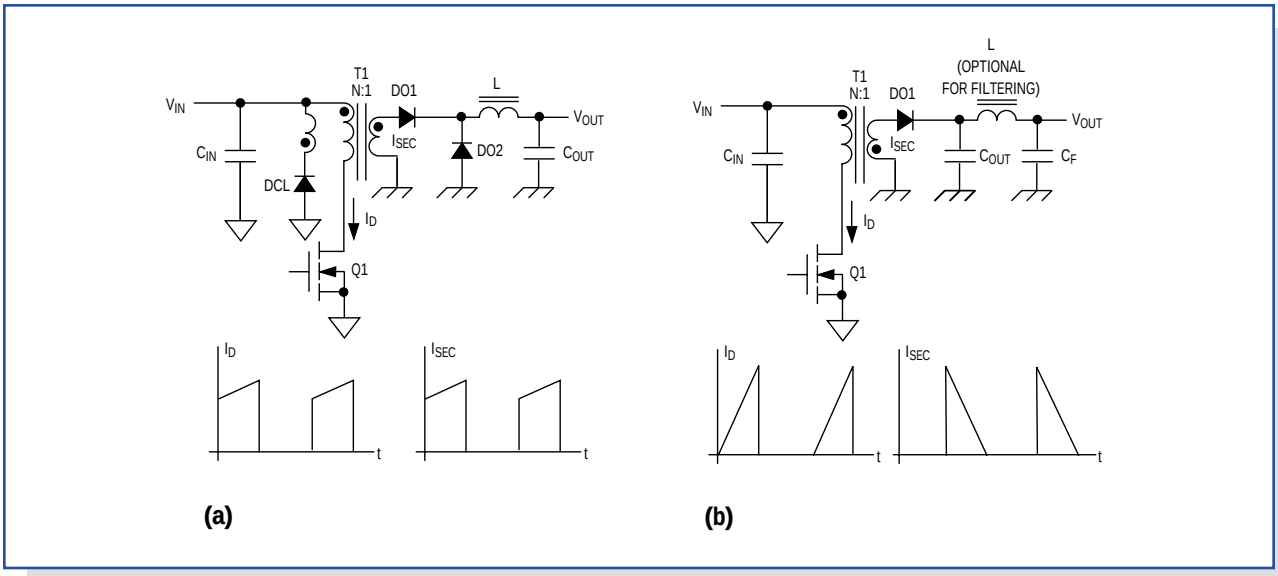


Figure 2. Forward and flyback power topologies

Figures 2a and 2b show a forward and flyback converter. Figure 2a shows the power-stage configuration of a forward converter. Power transfer to the secondary side circuit takes place when the power switch (Q1) is turned on. Almost all forward supplies are operated in continuous conduction mode, which means that the inductor energy is not completely depleted before the start of the next cycle. The drain current (I_D) looks rectangular, with a slight pedestal. DO1 reverse biases when Q1 turns off and DO2 forward biases, carrying the entire inductor current. The reset winding connected to the cathode of DCL allows for recycling of the energy stored in the transformer core by returning it to the input source.

Figure 2b shows the power stage of a flyback converter. In this case, power transfer to the secondary takes place after Q1 has turned off. Energy stored in the transformer core is delivered to the load. Flyback converters tend to cost less for lower power applications since they don't require an output inductor. A small filtering inductor is sometimes used, however, to reduce high-frequency spikes that are present at the output voltage. Flyback converters are often operated in discontinuous mode, which means that the energy stored in the transformer is completely transferred to the output before the start of the next cycle.

instantly responding to varying input voltages and correcting the duty cycle within a single cycle without the intervention of the slower voltage control loop.

The following should help clarify the effect of feedforward compensation. The modulator and power-stage gains of a forward converter without feedforward compensation are given in Equations 1 and 2, respectively:

$$\frac{d}{V_C} = k_1 s_r \qquad (1)$$

where d is the duty cycle, V_C is the control voltage present at the PWM comparator input (pin 7), k_1 is a constant, and s_r is the slope of the internal modulating ramp:

$$V_{OUT} = k_2 d V_{IN} \qquad (2)$$

where k_2 is a constant, V_{OUT} is the output voltage, and V_{IN} is the input voltage.

The combination of Equations 1 and 2 results in Equation 3, which is the known ideal gain expression for forward and buck type regulators. However, in this expression, notice that the power-stage gain (V_{OUT}/V_C) depends on the input voltage:

$$V_{OUT} = k_1 k_2 d V_{IN} s_r V_C \qquad (3)$$

This dependence of power stage on the input voltage limits the attainable control-loop bandwidth in systems where the input voltage is subject to wide variations. Also, any fast perturbation on the input voltage line directly affects the output voltage as seen in Equation 3. The only correction

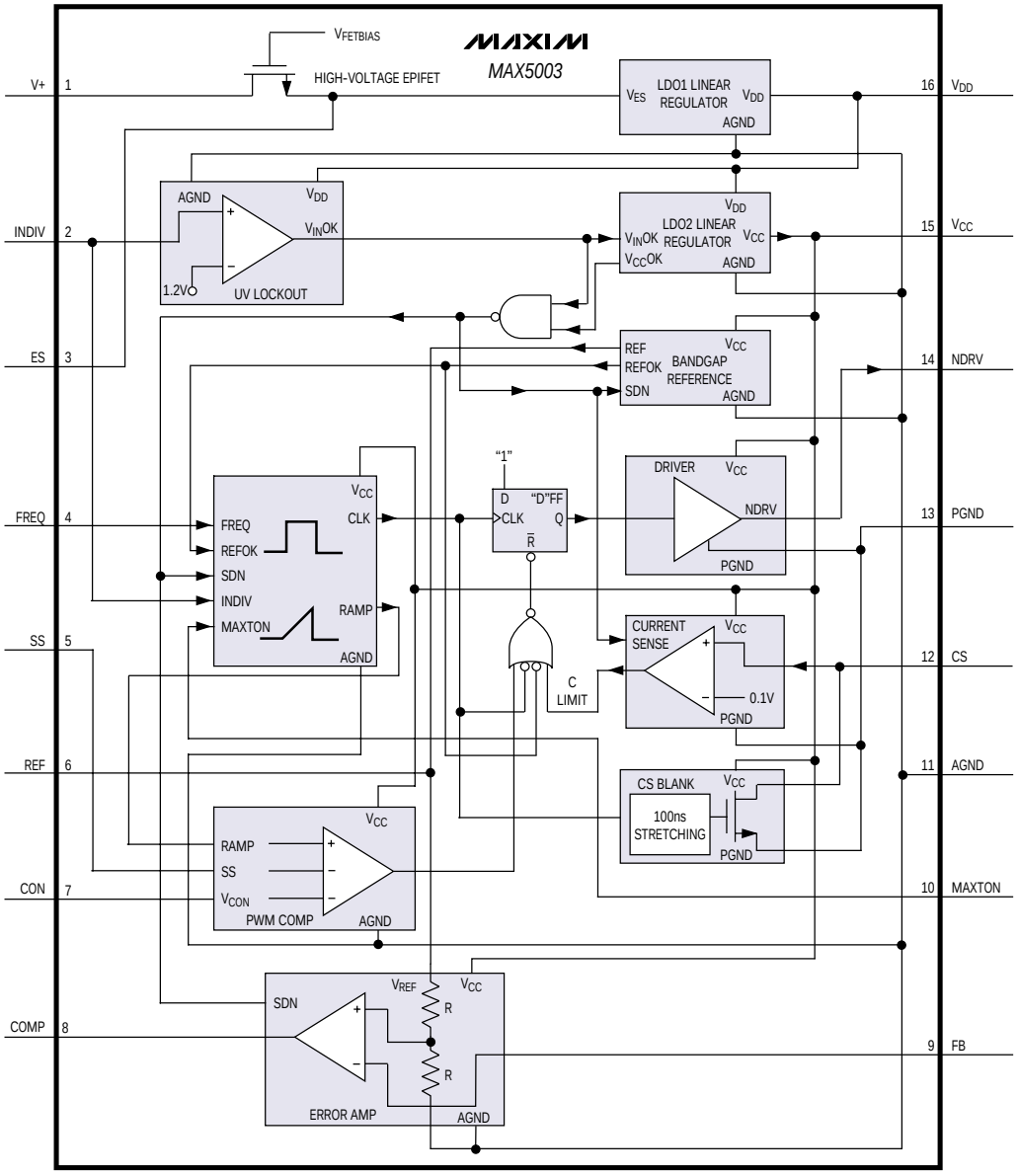


Figure 3. MAX5003 block diagram

to such perturbation (to keep the output voltage constant) must come from changing V_C, which entails the intervention of the relatively slow voltage error amplifier.

In a feedforward compensated system, the slope of the regulating ramp is made inversely proportional to input voltage as given by Equation 4:

$$s_r = \frac{k_3}{V_{IN}} \qquad (4)$$

By substituting Equation 4 in Equation 3, the constant gain expression of Equation 5 is obtained:

$$V_{OUT} = k_1 k_2 k_3 V_C \qquad (5)$$

From Equation 5, it is clear that the dependency of the output voltage on the input voltage has been completely eliminated; virtually all input voltage transients are rejected by the power circuit even without the intervention of the output voltage control loop.

The switching frequency is set by using an external resistor, and it has been set to 250kHz, which helps to minimize the size of the energy storage components without a big switching power loss penalty.

Forward converters with a reset winding (terminals 3 and 4 of the transformer) must have their maximum duty cycle clamped to specific levels to avoid transformer core saturation due to insufficient core reset. In general, the following condition must always be met to prevent transformer core saturation:

$$V_{IN}d \le V_{IN}\frac{N_{12}}{N_{34}}(1-d) \qquad (6)$$

where N_{12} and N_{34} are the number of turns of the main and reset windings.

Written in a simplified form, Equation 6 sets the required condition for the duty cycle. Then by solving for d, you can obtain Equation 7:

$$d \le \frac{N_{12}N_{34}}{N_{34}(N_{12}+N_{34})} \qquad (7)$$

The MAX5003 provides for maximum duty cycle limit by programming the MAXTON pin with a single resistor, thus helping to meet the above condition for an optimized design.

Telecom-grade power supplies also require an undervoltage lockout function. This is used to disable the power supply if the input voltage "drops" below a preset voltage (less than 32V in most systems). The undervoltage lockout threshold of this power supply is set by voltage divider R1/R2 (see Figure 1).

The startup circuit

The MAX5003 controller contains an internal high-voltage preregulator that directly connects to the input voltage. Power is fed from the V+ pin into a depletion junction FET preregulator. The preregulator drops the input voltage to a level low enough to feed a first low-dropout (LDO) regulator (Figure 3). The LDO input is brought out at the ES pin where it is decoupled with a small ceramic capacitor. The output of the primary side bias winding (T1-5 and T1-6) is rectified with D3 and applied to a voltage-level conditioning circuit comprised of R14, Q2, and Z1. This circuit limits the voltage level to a safe level so it can be applied to V_{DD}. The bias winding in this case operates in flyback mode, as opposed to the power stage that operates in forward mode. This eliminates the need for a filter inductor, thus saving cost. Energy to the winding in the flyback mode is supplied by the energy stored in the magnetizing inductance of the transformer during the on-time.

During initial startup, the first regulator generates the power for the V_{DD} line, which is available externally through a corresponding pin. Forcing voltages at V_{DD} above 10.75V disables the first LDO, turning off the high-voltage depletion FET, thus reducing the IC's power consumption, especially at high input voltages. Following the V_{DD} LDO is another regulator that drives V_{CC}—the power bus for the internal logic, analog circuitry, and external power MOSFET driver. This regulator is needed because the V_{DD} voltage level would be too high for the external N-channel MOSFET gate. The V_{CC} regulator has a lockout line that shorts the N-channel MOSFET driver output to ground if the V_{CC} LDO is not regulating. V_{CC} feeds all circuits except the V_{CC} lockout logic, the undervoltage lockout, and the power regulators.

The transformer

The key component in any isolated power supply is the power transformer. Critical power-transformer specifications that have a direct impact on efficiency and reliability are the primary and secondary winding DC and AC resistances, resulting in operating losses. The AC portion of the losses results from skin and proximity effects and, depending on the transformer (whether it is gapped or not), from circulating eddy currents. The proximity effect is the result of magnetic fields that distort the current flow in nearby winding conductors. The winding configuration plays a big role in these losses.

Another key parameter is leakage inductance, a critical parasitic element that must be kept as low as possible to maximize power transfer to the secondary. Low leakage inductance also reduces losses in the primary; in this design, some of the leakage energy is dissipated across Q1. **Figure 4** clearly shows the spike at the drain of Q1, briefly after turning off.

A less critical parameter is the magnetizing inductance. This is the inductance seen from primary terminals 1 and 2 with all other terminals open circuit. **Table 2** gives the transformer specifications.

The circuit of Figure 1 shows the electrical diagram of the transformer. The winding phase relationships noted with the dots next to the winding terminals are important.

The output circuit

The output uses a low-forward-drop, dual Schottky diode for high efficiency. This diode is rated to 20A,

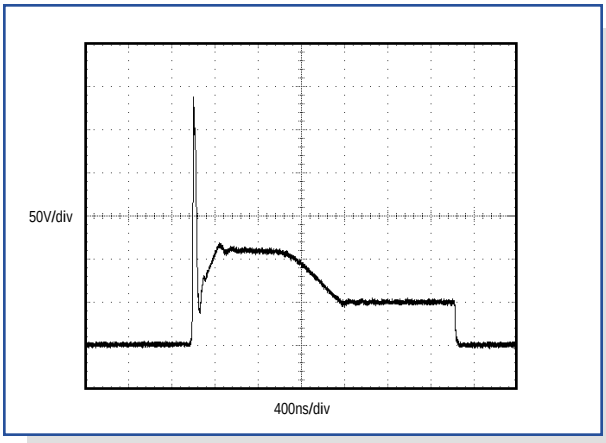


Figure 4. Q1, drain-source voltage waveform. Leading-edge spike results from the leakage inductance energy. This leakage energy is allowed to dissipate in Q1.

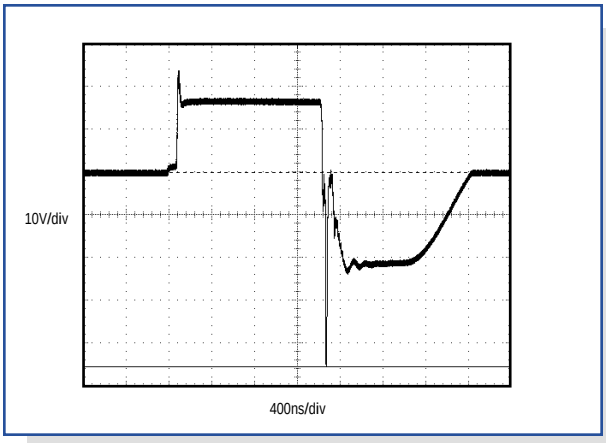


Figure 5. Waveform at transformer secondary

Table 2. Transformer specifications

Parameter	Specification
Primary turns (T1-1; T1-2)	14 Turns
Secondary turns (T1-8, 9; T1-11, 12)	5 Turns
Bias winding turns (T1-5; T1-6)	4 Turns
Reset winding turns (T1-3; T1-4)	12 Turns
Magnetizing inductance (T1-1; T1-2)	250µH
Leakage inductance	<1µH
Hipot secondary to any other winding	1500V for 1s
Core geometry	EFD20
Core material	High-frequency ferrite
Mounting	12-pin surface-mount bobbin

with a 40V reverse breakdown voltage adequate for this output. The total average current rectified by this diode is 10A, resulting in approximately 5.5W of power dissipation. As such, this diode needs to be cooled, with a heatsink capable of keeping the junction temperature at acceptable levels under worst-case ambient temperature conditions. **Figure 5** shows the output voltage at the secondary of the transformer. Notice the negative-going spike on this waveform. This spike's energy is small, and the diode is able to absorb this energy safely. Also, the R/C network (R13/C12) helps to reduce ringing at the secondary side.

In Figure 1, inductor L1 is capable of conducting 10A without significant losses. It is a 4.7µH high-current, surface-mount type. Although it is rated for higher currents, the low series resistance helps to keep losses low. Ripple current is approximately 2.2A peak to peak. Thus, the inductor current becomes discontinuous with an output current of approximately 1.1A.

The output capacitors can be either tantalum or aluminum electrolytic types. There are three primary considerations when selecting these capacitors: allowable AC ripple current handling, output voltage ripple, and (as it will be seen later) control-loop stability. When using low-cost electrolytics, additional low-value ceramic capacitors may be used to further reduce switching noise spikes at the output terminals. In this circuit, the expected AC RMS current through the capacitors is approximately $0.8A_{RMS}$; therefore, these capacitors should be sized to safely handle this level of ripple current.

The feedback circuit

In Figure 1, the two main elements of the voltage feedback circuit are the TL431 shunt regulator and the MOC207 optocoupler. **Figure 6** shows the internal block diagram for the TL431. Several manufacturers produce this part, which comes in various grades of accuracy. The internal reference voltage of the shunt regulator is 2.5V (typ). An external voltage-divider is used, consisting of R11/R12 for a 5V regulated output voltage. This feedback circuit configuration is very common in switching power supplies and is widely used. However, its operation is sometimes misunderstood, resulting in potential pitfalls.

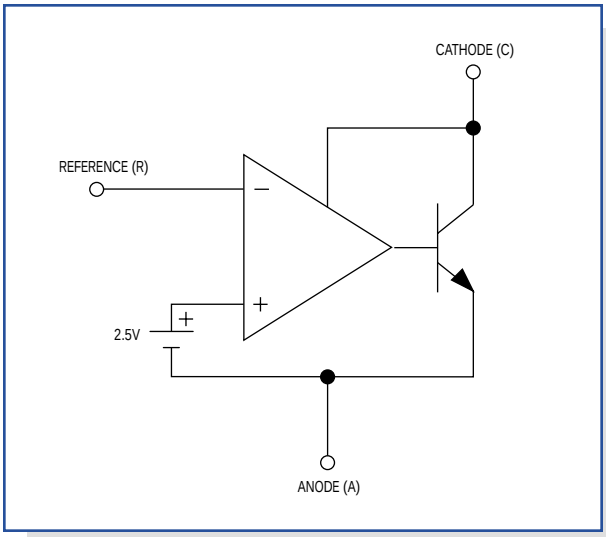


Figure 6. Simplified TL431 shunt regulator block diagram

This circuit has two feedback paths from the output. One path is through the shunt regulator providing the low-frequency gain for good output voltage regulation, whereas the second path is through the optocoupler itself to the cathode terminal of the shunt regulator. To visualize this latter loop, it suffices to replace the shunt regulator with a virtual constant-voltage source. In this arrangement, any increase in output voltage will result in a higher current flowing through the optocoupler LED, forcing the collector voltage of the coupled phototransistor to fall and thus reduce the duty cycle. This results in a negative feedback loop that has the tendency to keep the output voltage constant. Therefore, be careful when trying to stabilize this loop. The easiest method, and the one adopted in this design, is to rely on the equivalent series resistance (ESR) of the output capacitors for proper compensation of this latter feedback path. However, this puts a constraint on the minimum ESR value. The following formula provides a good rule of thumb for ESR:

$$ESR \cong \sqrt{\frac{L}{C}} \qquad (8)$$

ESR tolerances of ±30% should be suitable. Note, meeting Equation 8 in an otherwise well-designed system means that the phase margin at the unity-gain crossover point of the control loop approaches 90° for a rock-solid transient response.

Example:

$$ESR \cong \sqrt{\frac{(4.7\mu H)}{(330\mu F)}} \Rightarrow ESR \cong 120m\Omega \qquad (9)$$

Thus, to get the required ripple at the output, one or more capacitors may have to be paralleled. For a 50mV peak-to-peak voltage ripple at the output, four 330µF capacitors with an ESR of 90mΩ each can be used.

The compensation capacitor around the shunt regulator is not very critical in most cases, and its value can be around 0.1µF. Much lower values for this capacitor may reduce the control loop's overall phase margin.

The feedback circuit is completed in the primary by connecting the collector of the phototransistor in U2 to the MAX5003 CON input. Although the control IC contains an error amplifier, that amplifier is not used in this case. Still, this amplifier is very useful for non-isolated applications and where regulation is done through a biasing auxiliary winding connected to the primary side.

Input circuit

The input circuit consists of three ceramic bypass capacitors (C4, C5, C6). When embedding the power supply to an actual system, it is advisable to use bulk storage capacitors. These capacitors must be sized so they can safely handle the ripple currents present at the converter input.

$$I_{RMS} = I_P\sqrt{d_{50\%}(1-d_{50\%})} = 0.51_P \qquad (10)$$

where I_p is given by the following:

$$I_P = \frac{P_{OUT}}{\eta V_{IN(MIN)} d_{(MAX)}} \cong 3A \qquad (11)$$

Note that the worst-case ripple current through the input capacitor is around 50% duty cycle. For the circuit of Figure 1, the AC capacitor ripple current is $1.5A_{RMS}$. These capacitors should be placed very close to the input to keep long traces from carrying high-frequency switching currents that may cause EMI problems. Additional input filtering may be necessary to meet applicable regulations.

Key power-supply waveforms

Waveforms at the circuit's key points help explain the operation further. Figure 4 shows the switching FET's drain-source waveform. The initial spike results from the transformer's leakage inductance. This is much lower at lower output power levels. In this case, the FET absorbs the leakage energy.

Figure 7 shows the voltage pulse at the output of the secondary rectifier. This is a relatively clean waveform with minor leading and trailing edge spikes.

Figure 8 shows the well-behaved rise of the output voltage. The MAX5003's soft-start feature gradually increases the duty cycle, thus eliminating any potential overshoots during startup.

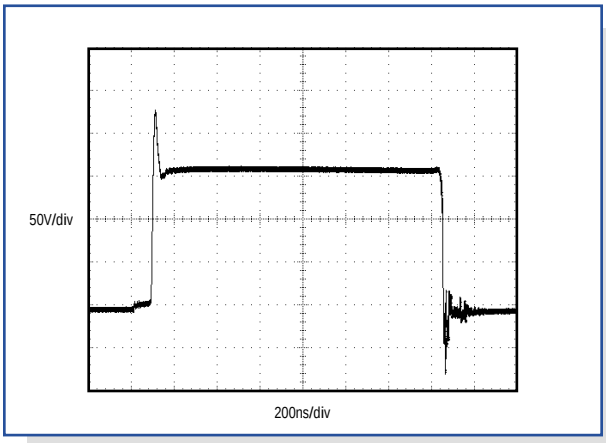


Figure 7. Waveform after output diode

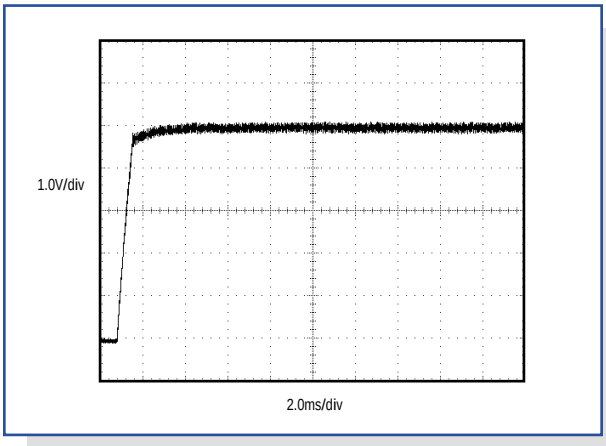


Figure 8. Output voltage turn-on transient at power-up (V_{IN} = 48V, I_{OUT} = 5A)

Power-supply performance

Key power-supply performance characteristics include efficiency and output voltage regulation curves. **Figure 9** shows the efficiency versus output power. The efficiency reaches 85% at about 25W of output power and stays relatively flat up to 50W. Even though the efficiency is very high, heatsinking is required for the power FET and output diodes. The diode will dissipate about 6W with a 10A output current, and the FET can be expected to dissipate about 3W to 4W. A slight airflow over the power supply will cool down the power transformer and output inductor.

Figure 10 shows the output voltage regulation of the power supply from 0 to 10A of output current. Voltage measurement was done at output voltage sense points. **Table 3** lists the power-supply performance specifications.

Table 3. Power-supply performance specifications

Parameter	Specification
P_{OUT}	50W
V_{IN}	+36V to +72V OR -36V to -72V
V_{OUT}	+5V
I_{OUT}	10A
Initial output voltage setpoint accuracy	±3%
Output voltage regulation measured over line and load	0.3%
Efficiency measured at 48V and 25W	85%
Input output isolation	1500V for 1s
Switching topology	Feedforward compensated forward
Dimensions	4.05in x 1.3in

Initial setpoint accuracy can be improved with external component trimming or by using a better tolerance output voltage sense-resistor divider.

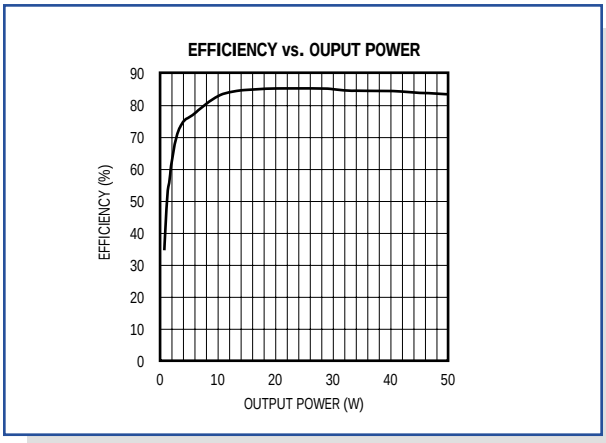


Figure 9. Efficiency curve

PC board layout and component placement

As for any other switching power supply, component placement is very important. Because of the primary-to-secondary isolation, the primary and secondary grounds are separated. **Figure 11** clearly shows the separation on both sides of the PC board. The board layout can be changed to accommodate different footprints. Also, the

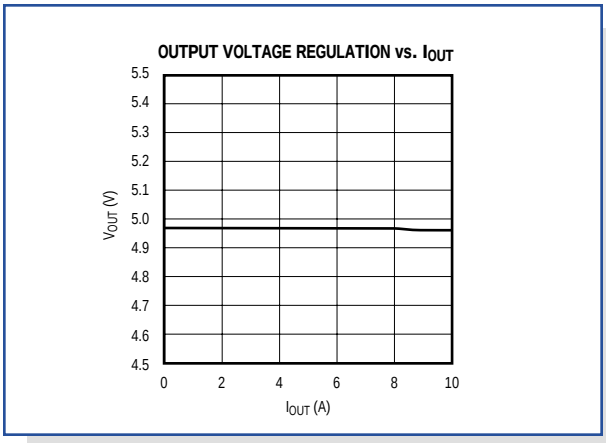


Figure 10. Output voltage regulation

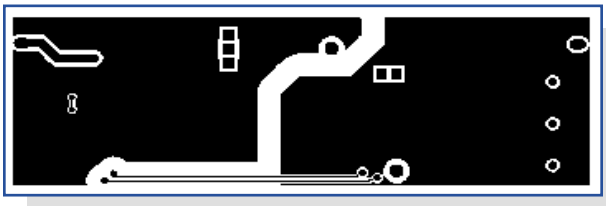


Figure 11. Bottom-side copper tracks of the FWD0510 power supply

power FET and output rectifier should be mounted on a heatsink for best thermal management. In this implementation, both of these components were mounted on the noncomponent side of the board, with their tabs exposed so they can be easily mounted on a heatsink.

The critical layout points are as follows:

- The distance from the secondary transformer leads to diode D4 should be kept to a minimum. This will improve EMI as well as the effective available power transfer.
- Bypass capacitors C4, C5, and C6 should be as close as possible to lead 1 of T1.
- Lead 2 of T2 should be as short as possible.
- Current-sense resistor R6 should be as close as possible to the source of Q1 and should return with a very short trace either to the ground plane or to the negative lead of bypass capacitors C4, C5, and C6.
- The gate drive loop of Q1 must either be routed over the ground plane or should be very short.

All other components must be placed close to the control IC. Relevant trace spacings (relating to trace creepage) must be observed.

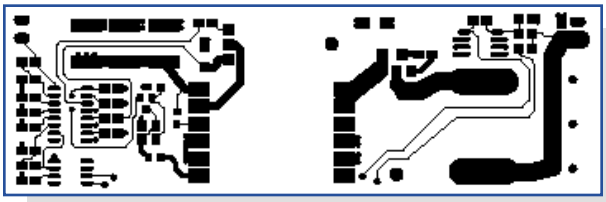


Figure 12. Top-side copper tracks of the FWD0510 power supply

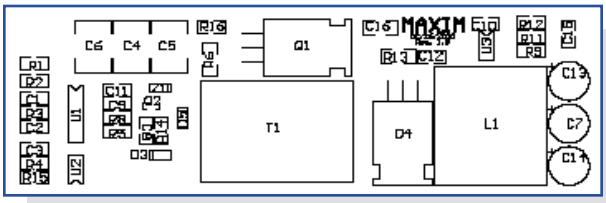


Figure 13. Component placement of the FWD0510 power supply. Note that Q1 and D4 are placed on the bottom side where their metal tabs are exposed to a heatsink plate.

IC equalizes gigabit copper-cable links

There is a growing need for short-distance, high-speed, serial data links for interconnecting communication systems. Until now, most chassis extensions and rack-to-rack connections exceeding 20ft relied on copper cable and offered rates of 1Gbps or less. Some links operate at 2.5Gbps over copper but only for distances of 10ft or less. All other links at 2.5Gbps rely on optical transmission for 50ft or more.

With the introduction of the MAX3800 adaptive cable equalizer, however, an inexpensive copper cable can handle 3.2Gbps up to 100ft. Although the MAX3800 is designed for compensating copper cable, it compensates circuit-board transmission lines as well. The following is a brief survey of MAX3800 performance with different cables and with a sample of FR4 PC board material.

Test setup

Figure 1 shows the setup used to evaluate MAX3800 performance with various cables. In each case, the applied pattern was a PRBS-7 with a 1Vp-p output level. The eye diagrams were acquired with a Tektronix CSA8000 oscilloscope. The CSA8000's FrameScan™ feature was used to reduce random jitter, allowing a direct measurement of deterministic jitter.

Cables

The four cables evaluated range in cost from a few pennies per foot to tens of dollars per foot. An expensive matched set of 50Ω coaxial cables from W.L. Gore, which guarantees the loss characteristics for skin and dielectric, was used as a laboratory reference. Most cable manufacturers do not attempt to specify loss characteristics except for a few points where losses are insignificant. After all, most users are interested in the cable's low-loss frequency range. Still, without detailed cable characteristics, it is difficult to predict the performance of an equalizer. The testing of these samples is intended to assist in cable selection.

The 100ft RG179B is 75Ω cable used to drive the MAX3800 equalizer in single-ended fashion. No matching network was used to adapt between the 50Ω and 75Ω environments. (For such a long length of cable, reflections are greatly attenuated by the cable and therefore pose no problem to the equalizer.)

The 100ft Belden 9207 is 100Ω twin-axial cable consisting of 18AWG conductors and a heavy-duty protective casing.

The inexpensive Madison 14887 is shielded, twisted-pair 100Ω cable. Intended for use in LVDS applications, it is an extremely light-weight cable with 30AWG conductors. As a convenience for multichannel interconnects, it can be ordered in multipaired bundles. Similar cables are available from Amphenol and Tensolite.

Finally, the FR4 circuit board sample is a 50Ω transmission stripline 50in long and 6mils wide, driven as a single-ended load with 500mVp-p at the pattern generator.

Results

Table 1 lists length, bit rate, and deterministic jitter for the samples described above. **Figure 2** shows that the MAX3800 equalizer can restore high-frequency information that is 30dB down. The upper trace is the cable output applied to the MAX3800 input, and the lower trace is the fully restored signal at the MAX3800 output. **Figures 3–6** illustrate eye diagrams for the four cables operating at 2.5Gbps. **Figures 7** and **8** are eye diagrams for the FR4 transmission line.

Table 1. Equalized cable performance

Medium	Length (ft)	Bit Rate (bps)	Deterministic Jitter (UI)
W.L. Gore type-89 matched 50Ω coax pair	115	3.2G	0.04
		2.5G	0.03
		622M	0.01
RG179B coax single-ended 75Ω	100	3.2G	0.16
		2.5G	0.09
		622M	0.04
Belden 9207 twin-axial 100Ω	100	3.2G	—
		2.5G	0.20
		622M	0.04
Madison #14887 shielded, twisted pair 100Ω	50	3.2G	0.16
		2.5G	0.12
		622M	0.02
Stripline, FR4 6mil-wide, 50Ω	4.2 (50in)	3.2G	0.09
		2.5G	0.06
		622M	0.03

FrameScan is a trademark of Tektronix.

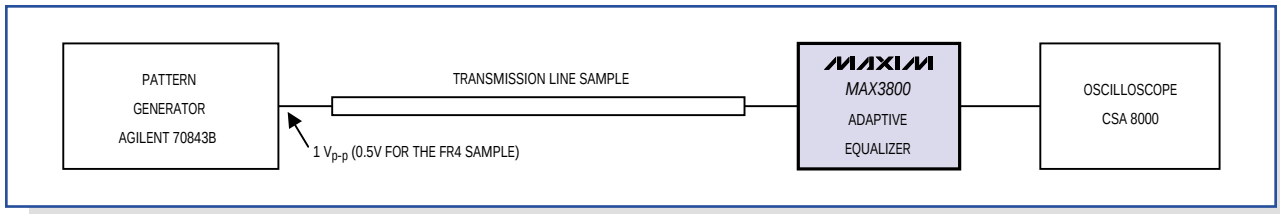


Figure 1. This test setup was used to measure MAX3800 performance using four different cables. (When using single-ended lines, the unused input to the MAX3800 should be AC-terminated to the same impedance as the transmission line.)

Conclusion

Equalizing gigabit signals with the MAX3800 offers new possibilities for data distribution and interconnection in a world starving for more bandwidth.

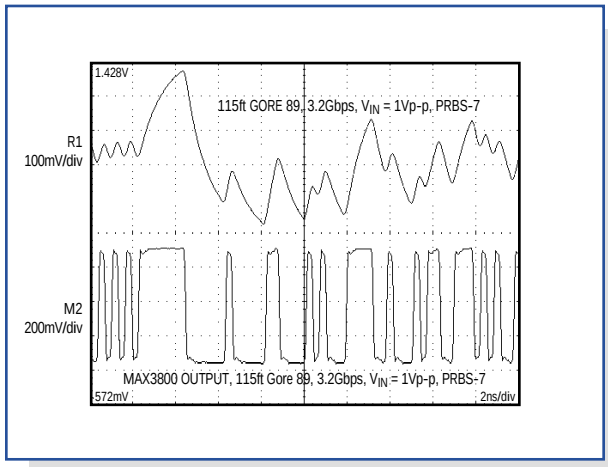


Figure 2. These before-and-after equalization waveforms show a 1Vp-p signal after travelling through 115ft of Gore type-89 cable (top trace). Note the small ripples and bumps, which represent single bits that have encountered 30dB of loss. The MAX3800 output (bottom trace) restores all bits.

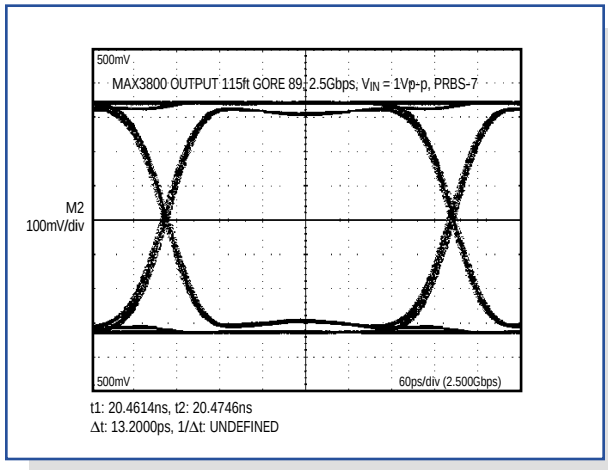


Figure 3. Restored by the MAX3800 after 115ft of Gore type-89 cable, the 2.5Gbps signal exhibits only 13ps of deterministic jitter.

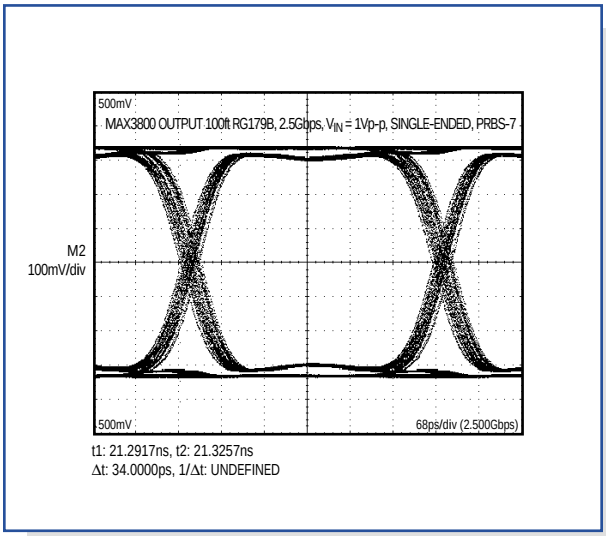


Figure 4. Restored by the MAX3800 after 100ft of 75Ω RG179B cable, the 2.5Gbps signal exhibits 34ps of deterministic jitter.

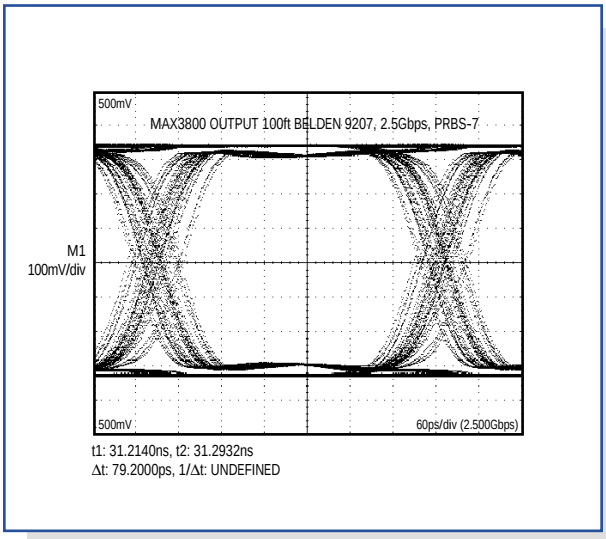


Figure 5. Restored by the MAX3800 after 100ft of 100Ω twin-axial cable, the 2.5Gbps signal exhibits 79ps of deterministic jitter.

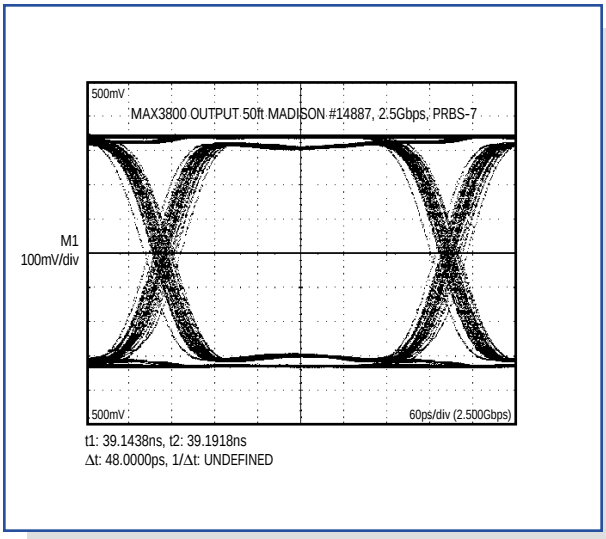


Figure 6. Restored by the MAX3800 after 50ft of 100Ω twisted-pair cable, the 2.5Gbps signal exhibits 48ps of deterministic jitter.

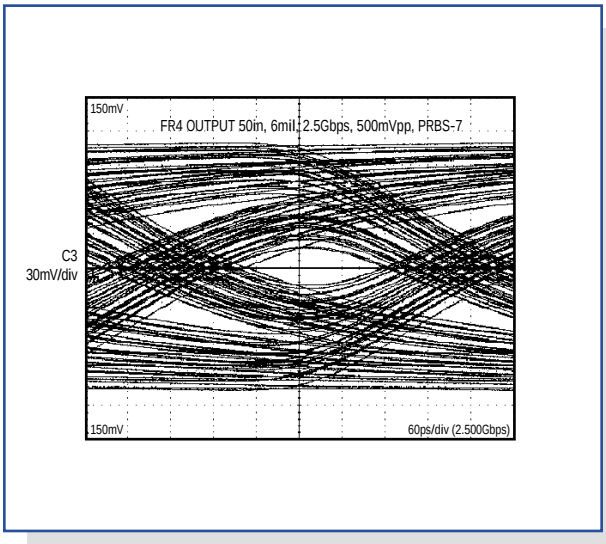


Figure 7. Before equalization, this 2.5Gbps signal at the MAX3800 input had travelled 4.2ft (50in) over 6mil-wide, 50Ω stripline. The eye is nearly closed, with a vertical opening of less than 30mVp-p.

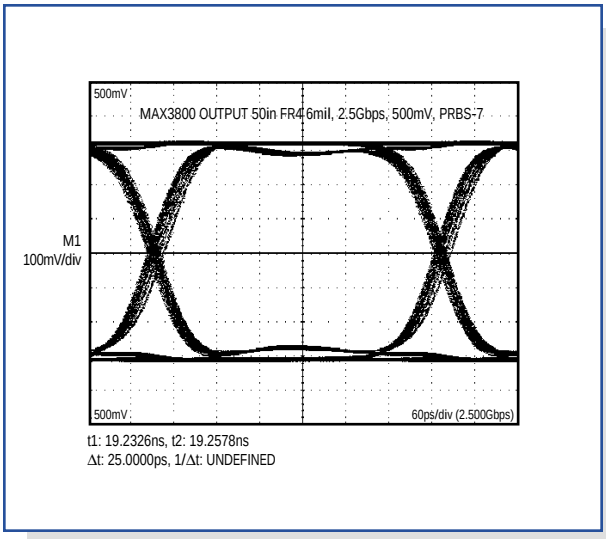


Figure 8. After restoration by the MAX3800, this Figure 7 signal (now at the MAX3800 output) has only 25ps of deterministic jitter.

DAC/µP-supervisor combination improves analog I/O reliability

The analog control signals used in industrial controllers, programmable-logic controllers (PLCs), and data-acquisition systems include 0 to 5V, 0 to 10V, ±5V, ±10V, and 4-to-20mA current loops. For safety reasons, some analog-output modules employ optocouplers to isolate electrically the microprocessor (µP) and analog circuits. Also, for reliability and safety, other systems require that the analog outputs reset to midscale or zero in response to a µP failure.

These requirements are met by the **Figure 1** circuit, which monitors µP activity and sets the analog output to zero when it detects a µP failure or undervoltage condition. It also improves the mean time before failure (MTBF) by minimizing I/O pins at the µP and by eliminating an optocoupler.

Three DAC (U2, MAX5120BEEE) features enable the circuit to produce zero-scale resets: an asynchronous-reset input (CLR), a user-selectable reset-value input (RSTVAL), and a user-programmable output (UPO) for serial-interface setup. These built-in features also eliminate an optocoupler, minimize I/O pins at the µP, and minimize the need for external discrete circuitry. The µP supervisor (U3, MAX6303CUA) includes a resistor-programmable reset input threshold, a capacitor-programmable watchdog timer, and a reset timeout period.

As DAC codes range from 000hex to FFFhex, the circuit output (V_{OUT}) ranges from -10V to +10V. Op amp U1A is offset by the DAC's internal 10ppm/°C precision bandgap reference, and output op amp (U1B) is configured as a buffer with a gain

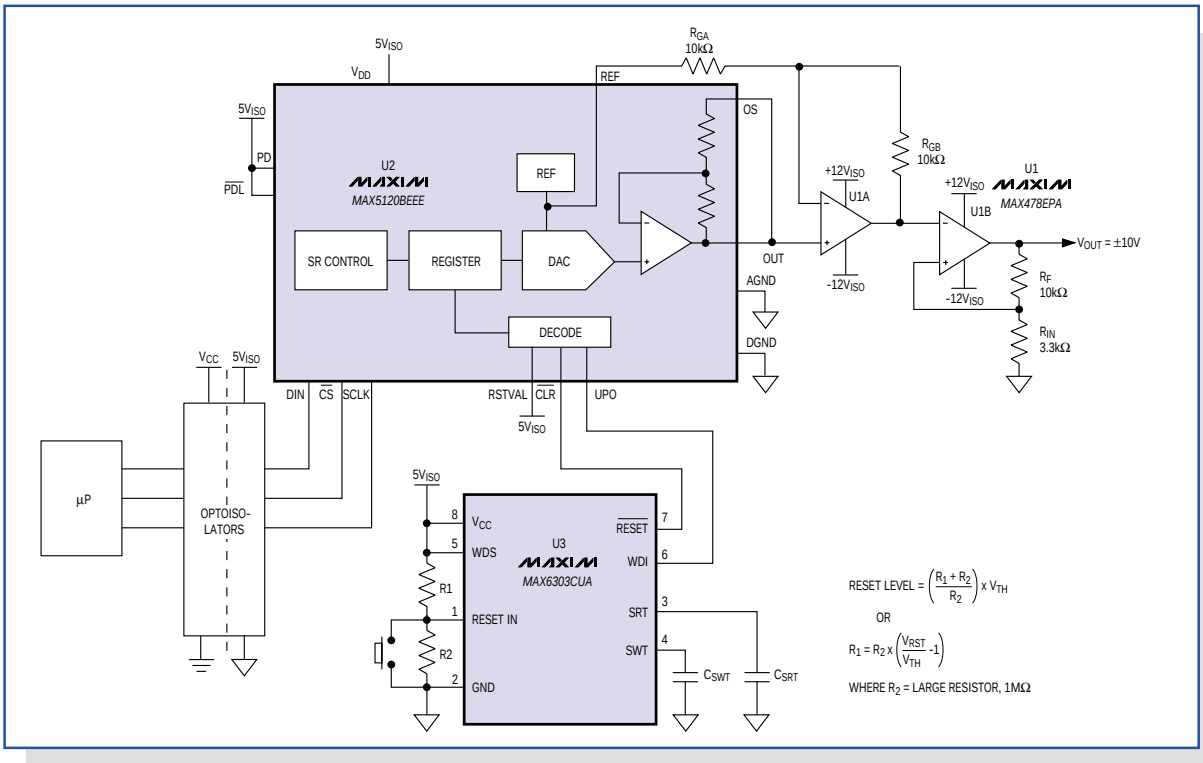


Figure 1. When a failure occurs in the supply voltage or µP operation, this DAC (U2) and µP supervisor (U3) together produce a user-programmed default output (V_{OUT}).

of four. Output voltage for the circuit is:

$$V_{OUT} = V_{REF} \times (G \times NB/4096 - 1) \times (R_F/R_{IN} + 1)$$

where NB is the numeric value of the DAC's binary code, V_{REF} is the internal reference voltage, G is the gain of U1A, and R_F/R_{IN} is U1B's gain-resistor ratio.

U3 (MAX6303CUA) monitors the isolated supply voltage (V_{ISO}) through its V_{CC} pin. It also monitors µP activity through its WDI pin and generates a reset command through RESET. A resistor-divider at RESET IN (pin 1) determines the reset-level threshold (V_{TH}). Similarly, the reset timeout period (t_{RP}) and watchdog timeout period (t_{WD}) are determined by capacitor values at SRT and SWT. Connect WDS to V_{CC} to enter extended mode, lengthening t_{WD} by a factor of 500. The following equations calculate values needed in the circuit:

$$V_{RST} = V_{TH}(R1 + R2)/R2$$

where V_{TH} = 1.22V, and V_{RST} is the adjustable reset threshold voltage:

$$C_{RST} = t_{RP}/2.67$$

where C_{RST} is in pF and t_{RP} is in µs;

$$C_{SWT} = \frac{t_{WD}}{(500 \times 2.67)}$$

where C_{SWT} is in pF and t_{WD} is in µs.

If V_{CC} fails, or if the µP locks up and cannot toggle WDI, U3 asserts low on its $\overline{RESET}$ output, which resets U2 through its $\overline{CLR}$ input. This action resets U2's output to the condition set by RSTVAL (to midscale in this case, which produces 0V at V_{OUT}). When U2 is being updated, its UPO output toggles U3's WDI at intervals less than the nominal watchdog timeout. Other devices to consider for the watchdog function are the MAX6316 series and MAX6369 series, which offer fixed timeout periods in SOT23 packages.

The switch between U3's RESET IN and GND terminals allows the user to command an emergency shutdown. $\overline{RESET}$ pulls $\overline{CLR}$ high after the reset timeout, but the DAC output remains at midscale until updated. The DAC's unipolar and bipolar modes allow it to produce all the common analog-output control signals.

Industrial AC-switch debouncer isolates input and output

Modern programmable logic controllers (PLCs) for automated process-control systems have either 16 or 32 inputs and accept AC voltages in the 24VAC to 120VAC range. A single circuit (a relay for electrical isolation and an RC network with Schmitt trigger to provide debounced signals to the processor) can debounce all these signals in sequence (although some may not need a debounce), but that approach slows the processing of real-time data. Such debounce circuits also provide delay times that change with relay wear and capacitor aging. In the PLC program, you can employ a debounce timer for each input, but that technique also increases the program scan time while tying up valuable timers.

A solid-state, electrically isolated circuit (**Figure 1**) can debounce single inputs without slowing down the PLC module. Optoisolators U1 and U3 provide electrical isolation for the AC sources at input and output. U2 (MAX6816) is a CMOS switch debouncer whose output (a 4V logic high) appears following a fixed 40ms delay. A 63kΩ pullup resistor, connected internally between IN and V_{CC}, forms a voltage divider with R2. The R2 value is chosen to ensure a logic low (<0.8V) at IN when U1's optotransistor (connected as an emitter follower) is off.

The two LEDs in U1, which illuminate the phototransistor on alternate half cycles of the AC input current, have the effect of rectifying this current. Most optoisolator applications set the current-transfer ratio (CTR) large (>10) to ensure an accurate reproduction of the input signal. This circuit, however, sets the CTR less than 1, which ensures

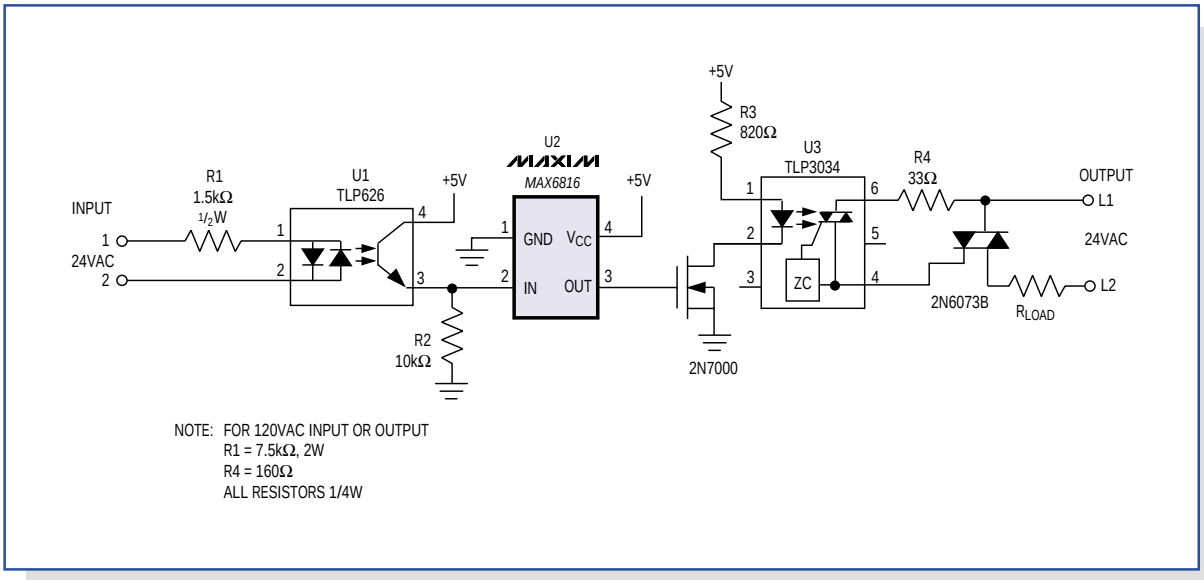


Figure 1. This AC-debouncer circuit enables an isolated AC voltage to control a separately isolated AC source.

that the emitter follower does not turn off completely as the AC current goes to zero twice in each cycle. R1 is chosen to bias the emitter follower such that U2's IN signal remains above the high level (>2.4V) during these zero crossings. This action eliminates the capacitor normally found in debouncing circuits.

U2's OUT pin drives the N-channel MOSFET, and R3 is selected so the resulting current flow (in MOSFET and LED) is about 5mA. When the MOSFET turns on, U3's zero-crossing triac driver is activated by the LED. Thus, when the power triac turns on, an AC source connected to the output drives R_{LOAD} with as much as 4A (**Figure 2**). Turning on the triac at zero crossings eliminates EMI and reduces the turn-on stress in that device. R4 is chosen to limit current into the triac driver (U3) to a maximum of 1A, and R_{LOAD} represents an electrical load such as the PLC inputs.

Each source can be either 24VAC (as shown) or 120VAC. For 120VAC inputs, change resistor values as noted on the schematic. This circuit is also useful in industrial relay-control logic to eliminate magnetic latching relays and provide precise AC-trigger pulses for relay timers.

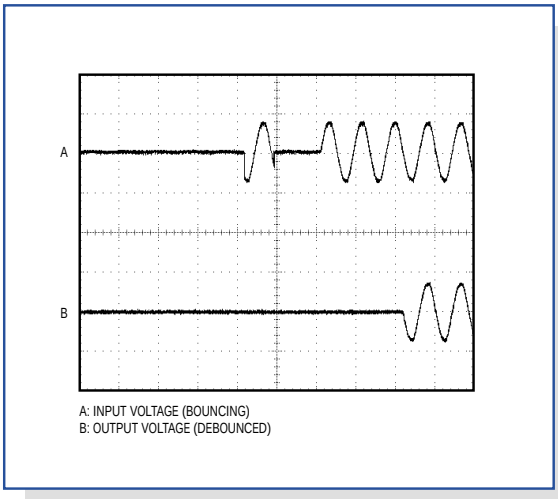


Figure 2. An AC switch (top trace) turns on and then bounces off briefly, while the output of the associated debouncer circuit from Figure 1 turns on cleanly (lower trace).

Multiplexer enables pseudo-multidrop RS-232 transmission

RS-232 communications with one microcontroller (µC) and more than one remote system can pose a problem because most µCs contain only one universal asynchronous receiver/transmitter (UART), which provides an interface between synchronous and asynchronous ports. The multiplexer in **Figure 1** (IC2) enables multiple channels (four, in this case) to share a single UART.

The dual 4-to-1 multiplexer (MAX399) allows transceiver IC1 (MAX3221) to form a network with the four remote transceivers IC3–IC6 (MAX3221E). **Table 1** defines the channel-selection codes. Selecting channel 1, for instance, enables IC1 to communicate with IC3 without being loaded by IC4, IC5, and IC6. Pulldown resistors internal to the remote transceivers force the outputs of unselected receivers to a known state.

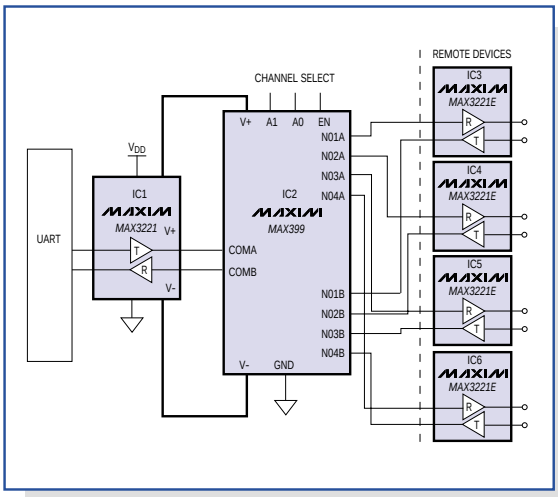


Figure 1. One UART and a multiplexer (IC2) enable one RS-232 transceiver (IC1) to communicate with four others in a pseudo-multidrop configuration.

Its supply-voltage range (3V to 5.5V) makes the Figure 1 circuit compatible with 3V and 5V logic. IC2 is powered directly from the V+ and V- terminals of IC1, whose ±5.5V outputs are generated by an internal charge pump. The multiplexer handles Rail-to-Rail® signals, so obtaining its power from IC1 ensures that RS-232 signals pass directly through, regardless of amplitude.

Each transceiver's charge pump requires four small capacitors (not shown), whose values depend on the V_{DD} range but do not exceed 0.47µF. Note that pulling too much current from the charge-pump terminals of IC1 (V+ and V-) will cause these rails to droop and may pull the IC's RS-232 transmission levels out of specification.

Table 1. Channel Selection

A1	A0	EN	Selected Channel
X	X	0	All channels disconnected
0	0	1	Channel 1 (IC3)
0	1	1	Channel 2 (IC4)
1	0	1	Channel 3 (IC5)
1	1	1	Channel 4 (IC6)

X = Don't care

Rail-to-Rail is a registered trademark of Nippon Motorola, Inc.

Solid-state circuit converts temperature to voltage

The circuit in **Figure 1** is a solid-state thermometer suitable for measuring temperatures from -40°C to +125°C. By adjusting R_{ZERO} and R_{SCALE}, you can calibrate and offset the output voltage (V_{OUT}) in accordance with any temperature scale. Celsius, for instance, requires an output change of 10mV/°C. You therefore adjust R_{ZERO} for 0.0V at 0°C, and R_{SCALE} for -100mV at -10°C.

The integrated temperature sensor (IC1, MAX6577) has a square-wave output whose frequency is proportional to its absolute temperature. To make use of this signal, the circuit employs a phase-locked loop (PLL) integrated into the waveform generator IC2 (MAX038). Because IC2 provides linear frequency tuning, its phase-detector output (PDO) is proportional to the input frequency and hence to temperature. Phase lock is accomplished by applying the PDO output to the frequency-adjust input FADJ. Because IC2's VCO gain is negative, an external op amp is provided to invert the final output voltage.

To calibrate, set the ambient temperature to 0°C (or 0°F), and adjust R_{ZERO} until V_{OUT} = zero. Then, set the ambient to room temperature (+25°C), and adjust R_{SCALE} until V_{OUT} corresponds to that temperature (to 250mV, for instance, if the scale is 10mV/°C). For a scale of 10mV/°C, the error versus temperature is less than ±1.5°C (**Figure 2**).

The temp sensor IC comes in a small 6-pin SOT23 package, so it is easily mounted on a PC board along with the other components. The thermometer's wide temperature range and small size are useful for both industrial and commercial applications.

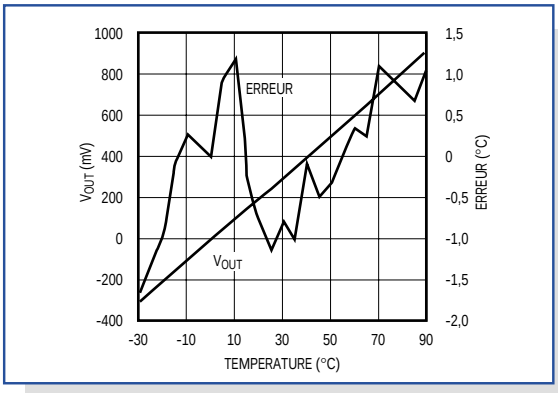


Figure 2. The output error for the Figure 1 circuit remains within ±1.5 °C.

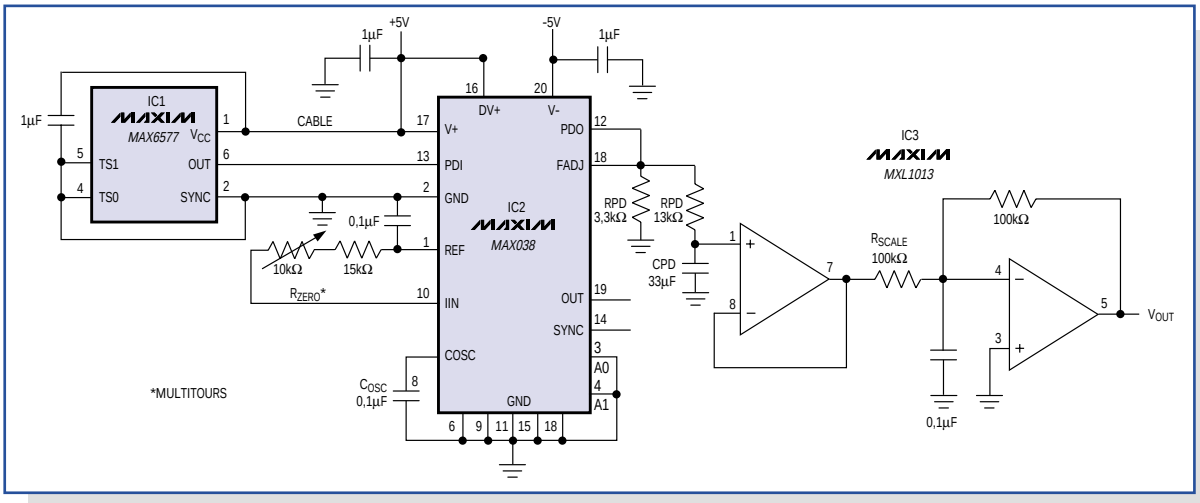


Figure 1. This three-IC circuit produces an output voltage proportional to the temperature of IC1.

Measuring threshold voltages

Most logic devices are characterized at 5V, but often you must know the upper and lower switching thresholds for a digital input operating at supply levels other than 5V. In some cases, you must also know the variation of these thresholds with supply voltage. A simple test circuit (**Figure 1**) enables these measurements to be made.

The basic idea is to create an oscillator by feeding an output signal back to the control input and monitoring the control input with an oscilloscope. You can then easily measure the upper and lower transition points on the scope. To slow the frequency of oscillation and reduce the effect of propagation delay, it can be desirable to add a capacitor, C1, as shown.

The circuit examines threshold voltages at the control input of an analog switch, but the scheme applies to any simple logic device. Switching thresholds for this IC depend on the logic-supply voltage applied to V_L. (The analog-switch channel COM-NO handles voltages in the ±15V range.)

The MAX4622 data sheet specifies IN thresholds for the most common usage (V_L = 5V), but the chip allows V_L to range from +4.5V to the positive rail, V+ (+15V in this case). This circuit characterizes the threshold voltages over the full operating V_L range (**Figure 2**). At power-up, the switch is open. V+ charges C1 through R1 and R2 until IN reaches its upper threshold, closing the switch. C1 then discharges to ground (through R2 and the switch) until IN reaches its lower threshold, thereby opening the switch and repeating the cycle.

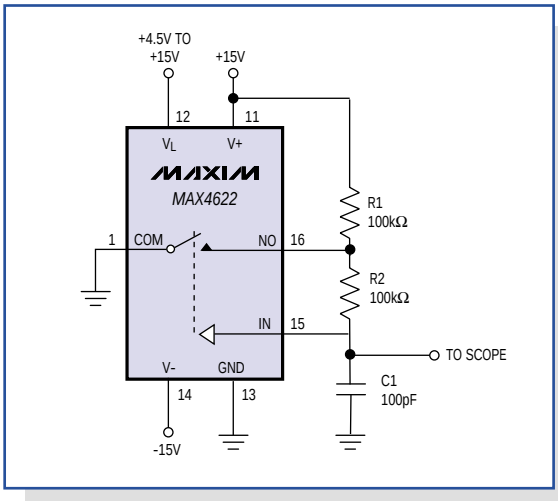


Figure 1. These external connections enable an oscilloscope to measure switching thresholds of any simple logic device, at any supply voltage.

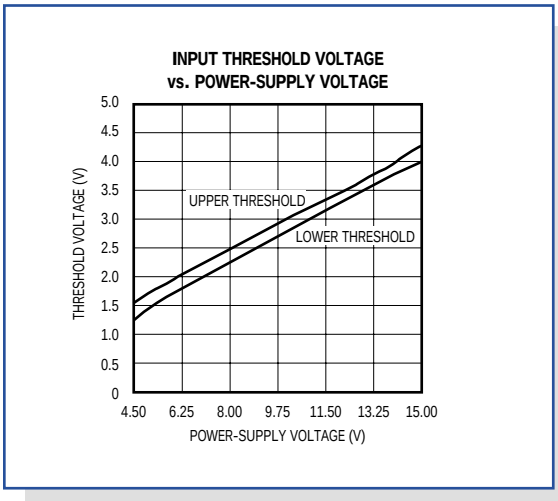


Figure 2. For the Figure 1 circuit, thresholds vary with supply voltage as shown (the supply voltage in this case is V_L at pin 12).

Notch filter is insensitive to component tolerances

Many approaches for creating notch filters (which reject a narrow band and pass all others) are less than satisfactory because they allow the component tolerances to interact. The **Figure 1** circuit overcomes this limitation and enables easy calculation of the component values for a desired notch frequency.

Two allpass filter stages (A1A and A1B, MAX4075) create a DC-accurate, 180° phase shift at the cutoff frequency. (The dual op amp [A1] includes gain resistors matched to within 0.1%—a tight tolerance that eliminates the need for trimming in most applications.) Summing this signal with the input produces a cancellation that produces the notch.

At very low frequencies for which the impedance of C2 is negligible, the circuit forms a voltage follower and produces no phase inversion. For high frequencies, however, this capacitor acts as a short circuit that causes the amplifier to act as a unity-gain inverter with its associated 180° phase shift. Phase behavior for the resulting allpass filter is identical to that of a single RC pole and produces 90° of phase shift at the resonant frequency (1/2πR1C1 or 1/2πR2C2).

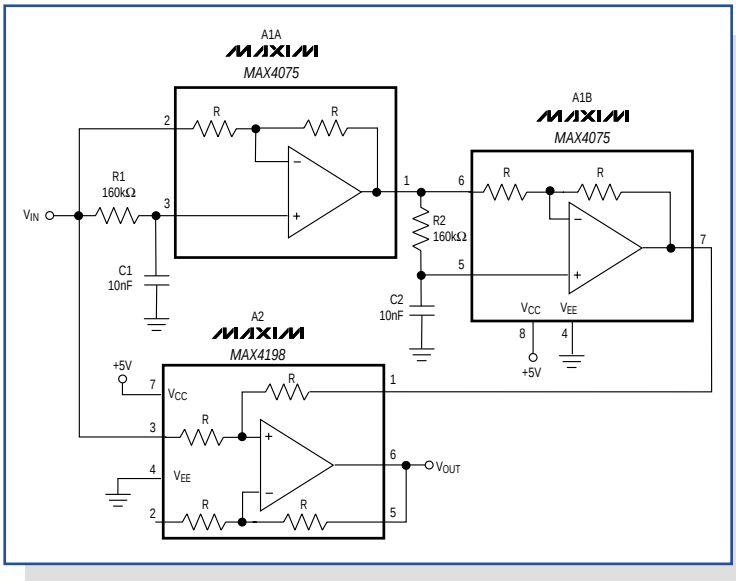


Figure 1. This circuit produces a notch-filter response by summing its input with the output of a dual op amp allpass filter (A1 and the associated components).

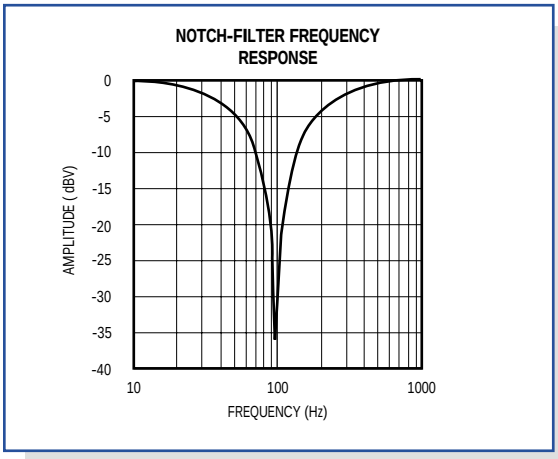


Figure 2. Operating the Figure 1 circuit with 5% resistors and 20% capacitors produces this response.

Components R1, R2, C1, and C2 affect only the notch frequency and not its depth. Conversely, the resistors integrated into dual-amplifier A1 affect only the depth of the notch and not its frequency. If you require a highly accurate notch frequency, specify R1, R2, C1, and C2 accordingly or simply trim one of the two resistors. A2 (MAX4198) is a precision differential amplifier used as a matched summing amplifier (note that the inverting input is left unconnected).

Circuit performance using 5% resistors and 20% capacitors, all unmatched, is shown in **Figure 2**. To produce a deeper notch, you can trim the circuit by adding a 100Ω resistor in series with pin 3 of A2 and a 200Ω potentiometer in series with pin 1 of A2. Adjust the pot for maximum rejection at the desired frequency.

Convert 5V to 1.8V without magnetics

To derive 1.8V from 5V, the first idea that comes to mind (perhaps) is a switch-mode regulator. Switchers are highly efficient but also complicated and expensive. Linear regulators are also out of the question, unless you can tolerate 36% efficiencies. The **Figure 1** circuit, on the other hand, is more than 70% efficient (**Figure 2**), sources up to 100mA, costs less than a switch-mode regulator, and requires less space.

IC1 (MAX660) is a CMOS voltage converter (charge pump) configured as a voltage inverter. With its output grounded and 5V applied to the V+ pin, it generates V+/2 = ~2.5V at pin 3 (GND). This nominal 2.5V output, which sags as the device sources current, is regulated to 1.8V by the linear regulator IC2.

IC2 (MAX8863) is capable of sourcing 100mA before its sagging input voltage falls below the dropout level (**Figure 3**). Using a larger value for C2 and C3 enables IC1 to maintain its output voltage for heavier load currents.

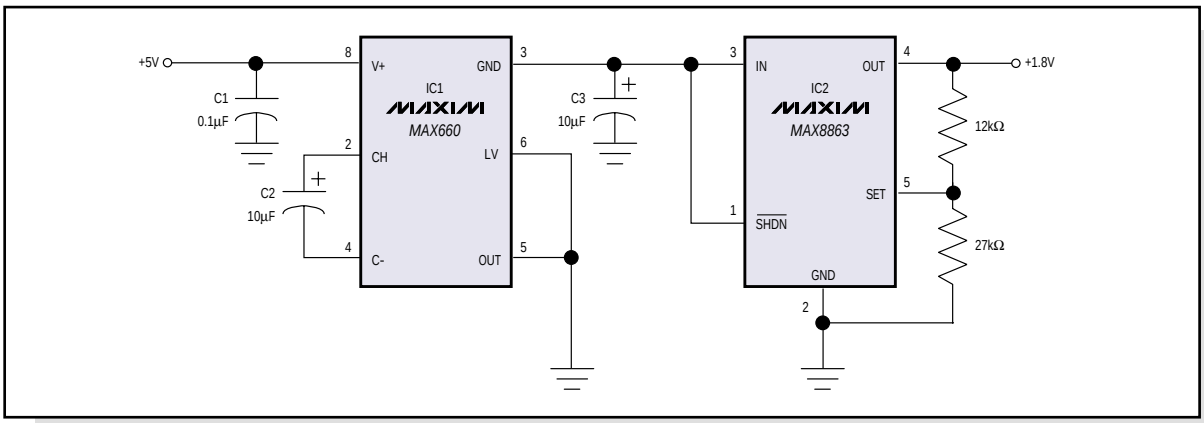


Figure 1. This "inductorless converter" lowers the input voltage with a charge pump before linear-regulating it to the desired output level.

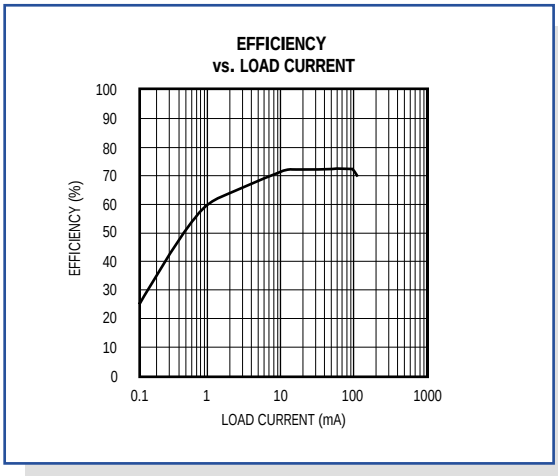


Figure 2. With the components shown, the Figure 1 circuit maintains its output voltage for load currents to 100mA.

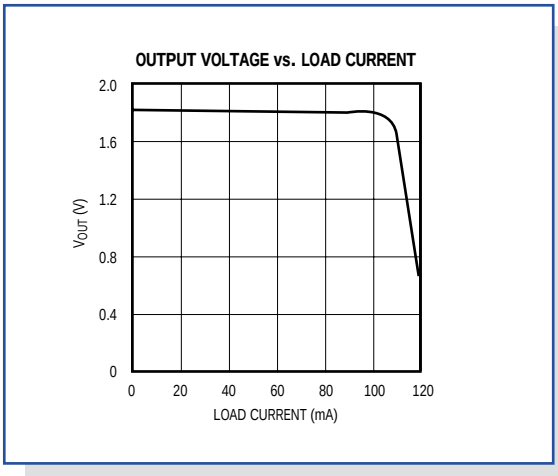


Figure 3. The Figure 1 circuit provides maximum efficiency for load currents between 10mA and 100mA.